

e filing Date : 8/27/2004

ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

Stylesheet Version v18.0

Title of Invention	METHODOLOGY OF QUANTIFICATION OF TRANSMISSION PROBABILITY FOR MINORITY CARRIER COLLECTION IN A SEMICONDUCTOR CHIP
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Application Number :

Confirmation Number:

First Named Applicant: Anne Watson

Attorney Docket Number: BUR920040120US1

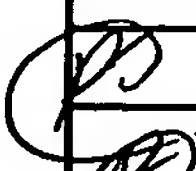




Art Unit: 2825

Examiner: P. KIK

Search string: (6493850 or 6553542 or 6490709 or 5559060 or 5638286 or 20030074641).pn


US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents


init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	6493850	2002-12-10	Venugopal et al.			
	2	6553542	2003-04-22	Ramaswamy et al.			
	3	6490709	2002-12-03	Kimura et al.			
	4	5559060	1996-09-24	Alsmeier et al.			
	5	5638286	1997-06-10	Fujimoto			

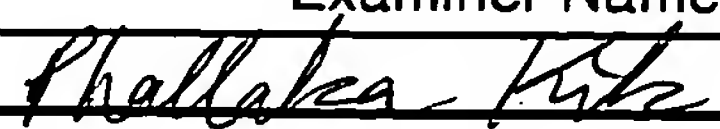
US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20030074641	2003-04-17	Kimura et al.			

Signature



Examiner Name	Date
	6/23/06

INFORMATION DISCLOSURE CITATION
(Use several sheets if necessary)

Docket Number (Optional)

BUR920040120US1

Application Number

10/711,143

Applicant(s)

A. Watson, et al.

Filing Date

August 27, 2004

Group Art Unit

2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
PD		JP2020039		Japan		abstract	✓	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

PD		SUBSTRATE MODELING AND LUMPED SUBSTRATE RESISTANCE EXTRACTION FOR CMOS ESD/LATCHUP CIRCUIT SIMULATION, T. Li, et al., Coordinated Science Laboratory, Dept. of Electrical and Computer Engineering University of Illinois at Urbana-Champaign, Urbana, IL (1999), 6 pages; 1999 ACM.
PD		BIPOLAR TRANSISTOR ACTION AND TRANSPORT EFFECTS RELATING TO CMOS LATCHUP, G. Krieger, IEEE Transactions on Electron Devices, Vol. ED-34, No. 8, August 1987, pgs. 1719-1728

EXAMINER

Phallabha Kik

DATE CONSIDERED

6/24/06

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>	Docket Number (Optional) BUR920040120US1	Application Number 10/711,143
	Applicant(s) A. Watson, et al.	
	Filing Date August 27, 2004	Group Art Unit 2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE


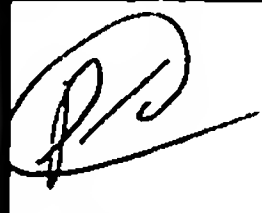
U.S. PATENT APPLICATION PUBLICATIONS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		PARASITIC LATERAL BIPOLAR TRANSISTORS IN CMOS, L. Deferm, et al., Solid-State Electronics, Vol. 32 No. 2, pgs 103-109, 1989.
		A NEW ANALYTICAL THREE-DIMENSIONAL MODEL FOR SUBSTRATE RESISTANCE IN CMOS LATCHUP STRUCTURES, M. Chen, et al., IEEE Transactions on Electron Devices, Vol. ED-33 No. 4 pgs. 489-493, April 1986.

EXAMINER <i>Phallake Kik</i>	DATE CONSIDERED <i>6/24/2006</i>
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INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>	Docket Number (Optional) BUR920040120US1	Application Number 10/711,143
	Applicant(s) A. Watson, et al.	
	Filing Date August 27, 2004	Group Art Unit 2825

U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		STATIC AND TRANSIENT LATCHUP SIMULATION OF VLSI-CMOS WITH AN IMPROVED PHYSICAL DESIGN MODEL, M. Strzempa-Depre, et al., IEEE Transactions on Electron Devices, Vol. ED-34 No. 6, June 1987, pgs 1290-1296
		A CMOS MODEL FOR COMPUTER-AIDED CIRCUIT ANALYSIS AND DESIGN, J. W. Roberts, et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 1, February 1989, pgs 128-138

EXAMINER Phallaka Hike	DATE CONSIDERED 6/24/2006
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INFORMATION DISCLOSURE CITATION
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Docket Number (Optional)

BUR920040120US1

Application Number

10/711,143

Applicant(s)

A. Watson, et al.

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U.S. PATENT APPLICATION PUBLICATIONS


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FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

OTHER DOCUMENTS

(Including Author, Title, Date, Pertinent Pages, Etc.)

		CORRELATING THE CHANNEL, SUBSTRATE, GATE AND MINORITY-CARRIER CURRENTS IN MOSFETs, C. Hu et al., IEEE International, Solid-State Circuits Conference, Digest of Technical Papers February 1983, pgs. 88-90

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6/24/06

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